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10/602,737	06/25/2003	Seiichi Nakatani	356972020512	1530

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MORRISON & FOERSTER LLP
1650 TYSONS BOULEVARD
SUITE 300
MCLEAN, VA 22102

EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,737	NAKATANI ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *37-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *37-49,51 and 52* is/are rejected.

7)☒ Claim(s) *50* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/196,792.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1004 & 0603*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

In the Preliminary Amendment, on p.2, the Applicant amended the Specification by inserting, as the first paragraph of the Specification, the continuity history to which the Applicant claims benefit under 35 USC § 120. The Examiner detected the following typographical and omission errors which should be corrected as follows:

(a) Change "09/956,511" to --09/956,551--.

(b) Insert –now U.S. Patent No. 6,625,037 B2-- after the comma following "2001".

Appropriate correction is required.

Regarding the IDS Form PTO-1449 filed 15 October 2004

2. PTO-1449 Ref. No. 8 is listed as "Japanese Office Action dated April 23, 2004." However, no such document has been scanned into IFW, made of record, or otherwise entered into the file. Accordingly, the Examiner has "lined-through" the above-cited entry. If the Applicant had intended to make this document of record, then the document should be submitted with Applicant's next communication with the Office or with Applicant's response to the present Office Action.

Claim Objections

3. Claim 52 is objected to because of the following informalities:

In Claim 52, there is no antecedent basis in base Claim 37 for "the conductive resin composition." However, there is antecedent basis in Claims 41 and 46. It appears that the Applicant had one of Claims 41 and 46 in mind as the claim from which Claim 52 was to depend. Accordingly, Applicant needs to change the dependency of Claim 52 from "37" to the appropriate claim (Claim 41 or 46) that provides the antecedent basis for "the conductive resin composition".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 39 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In Claim 39, the Applicant recites "wherein 70 wt % to 95 wt % of the mixture comprises the inorganic filler **and the thermosetting resin**." [Bold emphasis added]. There is no support in the disclosure for this limitation. However, there is support for *wherein 70 wt % to 95 wt % of the mixture comprises the inorganic filler* (see Specification, p.18, lines 10-14). Accordingly, this rejection may be overcome by simply deleting "and the thermosetting resin" in line 2 of Claim 39.

Rejections Based On Prior Art

6. The following references were relied upon for the rejections hereinbelow:

Kuritani et al. (JP05-299808 A)[†] Marrs (US 5,478,007)

Kiyooka et al. (JP04-018787 A)[‡]

[†]Submitted in IDS, filed 15 Oct 2004, and provided by the Applicant with a full English translation.

[‡]Submitted in IDS, 25 June 2003, and provided by the Applicant with only a partial English translation.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 37-39, 42-44, 46, 48, 49 and 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuritani et al. [*Examiner's Note*: The Examiner refers to the page and line numbers in the English translation of the above-cited Japanese document provided by the Applicant].

As to Claim 37, Kuritani et al. discloses, in Figs. 1a,c,d, a circuit component built-in module comprising: an insulating substrate 7 formed of a mixture comprising an inorganic filler and a thermosetting resin (p.6, lines 5-20); a plurality of wiring patterns 1

formed on at least one principal plane of the insulating substrate 7 (p.4, lines 30-33; p.5, lines 3-4 and 8-14); an active component 2 buried in the insulating substrate 7 and electrically connected to at least one of the wiring patterns 1 (Fig. 1c; p.5, lines 18-20); a passive component 2 buried in the insulating substrate 7 and electrically connected to at least one of the wiring patterns 1 (Fig. 1c; p.5, lines 18-22); wherein the active component is electrically connected to the passive component by the wiring patterns 1 (Figs. 1c and d depict a high-density modular circuit; p.9, lines 2-6).

As to Claim 38, Kuritani et al. further discloses an inner via (Fig. 1d) formed in the insulating substrate 7 and electrically connected to the wiring patterns 1 (Fig. 1d; p.6, lines 30-33).

As to Claim 39, Kuritani et al. further discloses that 70 wt % to 95 wt % of the of the mixture comprises the inorganic filler (p.6, lines 22-25; p.7, lines 10-29). In the example on p.7, the mixture comprises 950/1109 = 86 wt % of the mixture.

As to Claim 42, Kuritani et al. further discloses the circuit component 2 is shielded from external air by the insulating substrate 7.

As to Claim 43, Kuritani et al. further discloses the thermosetting resin comprises at least one of an epoxy resin, a phenol resin and a cyanate resin (p.6, lines 5-10).

As to Claim 44, Kuritani et al. further discloses the inorganic filler comprises at least one of Al_2O_3, AlN and SiO_2 (p.6, lines 15-19).

As to Claim 46, Kuritani et al. further discloses the wiring patterns 1 comprise at least one of copper (p.5, lines 3-7) and a conductive resin composition (p.5, lines 30-32;

the connective material--conductive resin, in this case--becomes a part of the wiring pattern that interconnects the components 2).

As to Claim 48, Kuritani et al. further discloses the circuit component 2 comprises at least one component selected from a chip resistor, a chip capacitor and a chip inductor (p.5, lines 18-22).

As to Claim 49, Kuritani et al. further discloses the mixture further comprises at least one additive selected from a dispersant, a coloring agent, a coupling agent and a releasing agent (p.7, lines 10-29).

As to Claim 51, Kuritani et al. further discloses the active component comprises a semiconductor bare chip 2, and the semiconductor bare chip is flip-chip bonded onto the wiring pattern 1 (p.5, lines 32-35).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 45 and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuritani et al.

As to Claim 45, Kuritani et al. discloses all the limitations of the claim except the limitation wherein an average particle diameter of the inorganic filler is 0.1 μm to 100 μm. However. Kuritani et al. does teach that "the particle diameter of the fillers may be any one as long as they do not clog the gate of the molding die" (p.6, lines 20-22). Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to limit an average particle diameter for the filler to a range of diameters that does not clog the gate of the molding die, including the range of diameters from 0.1 μm to 100 μm.

As to Claim 47:

Kuritani et al. discloses forming a wiring pattern in the copper foil disposed on the surface of the insulating substrate 7, including an embodiment (p.5, lines 8-10) wherein the copper foil is disposed on the entire side of the substrate (p.5, lines 3-10 and p.8, lines 18-19). In the embodiment wherein the copper foil is disposed on the entire side of the substrate, the Examiner takes Official Notice that the subtractive process of etching is an old and well-known process for forming a circuit pattern, and it would have been obvious to one of ordinary skill in the art at the time the invention was made to etch the copper foil after disposing it on the entire side of the substrate (p.5, lines 8-10) in order

to form the wiring pattern 1 (p.8, lines 18-19) that interconnects the active and passive components 2 on the insulating substrate 7.

12. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kuritani et al. in view of Marrs.

As to Claim 52 (the Examiner is assuming dependence from Claim 46 for referencing the antecedent "conductive resin composition"):

I. Kuritani et al. discloses that the active and passive components may be connected to the wiring pattern 1 by a conductive paste but does not specify the composition of the paste (p.5, lines 30-32).

II. Marrs discloses, in Figs. 5A and 8, connecting the active component 201 to a wiring pattern by a conductive resin 202, and that the conductive resin is an epoxy resin filled with silver particles (col.8: 55-62; col.9: 8-13; col.10: 1-4) for electrically connecting the active component 201 to the circuit substrate 501.

III. Since both Kuritani et al. and Marrs connect an active components to a wiring pattern on a circuit substrate using a conductive paste, the use of a conductive epoxy resin paste with silver particles, as taught by Marrs, would have been readily recognized in the pertinent art of Kuritani et al. as a useful conductive paste, for at least the reason that conductive resin pastes have a lower curing temperature than eutectic solder reflow temperatures 37%Sn/63%Pb solders (compare col.9: 35-51 and col.10: 51-57), which would be a benefit for electrically connecting temperature-sensitive active components.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the conductive paste of Kuritani et al. with the

silver particle filled conductive epoxy resin paste of Marrs et al. to effect reliable connection of the active component to the wiring pattern of Kuritani et al., as taught in Marrs.

13. Claims 37-44, 46, 48 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyooka et al. in view of Kuritani et al.

[*Examiner's Note*: The Examiner refers to the page and line numbers in the partial English translation of the above-cited document provided by the Applicant].

As to Claim 37:

I. Kiyooka et al. discloses, in Figs. 1e and 2, a circuit component built-in module comprising: an insulating substrate (38, 46) formed of a thermosetting resin (36, 44) (p.1, final paragraph); a plurality of wiring patterns (37, 45) formed on at least one principal plane of the insulating substrate (the sentence bridging pp.1-2; and p.2, lines 1-10); an active component (33b,c, 42a,b) buried in the insulating substrate (38, 44) (Fig. 2; p.1, second paragraph, lines 1-5; p.2, first full paragraph, lines 1-5) and electrically connected to at least one of the wiring patterns (37, 45) (through jumper chips 34 and 43 and anisotropic material 47; Fig. 2 and first full paragraph, lines 5-15); a passive component 33a buried in the insulating substrate 38 (Fig. 2; p.1, second paragraph, lines 1-5) and electrically connected to at least one of the wiring patterns (37, 45) (through jumper chips 34 and 43 and anisotropic material 47; Fig. 2 and first full paragraph, lines 5-15); wherein the active component (33b,c, 42a,b) is electrically connected to the passive component 33a by the wiring patterns (37, 45) (through jumper chips 34 and 43 and anisotropic material 47.

II. Kiyooka et al. does not appear to disclose (at least in the partial English translation provided by the Applicant) that insulating substrate (38, 46) is formed of *a mixture* comprising the thermosetting resin (36, 44) **and** *an inorganic filler.*

III. Kuritani et al. discloses an insulating substrate 7 formed of a mixture comprising a thermosetting resin (p.6, lines 5-10) and an inorganic filler that allows "the enhancement of thermal conductivity and the matching of thermal expansion of coefficient (CTE) with the inserted components" (p.6, lines 15-20).

IV. Since Kiyooka et al. inserts components 33a,b,c and 42a,b into the substrate resin (36, 44), then the use of inorganic filler that enhances thermal conductivity and match CTE with that of the components in order to ensure reliable package performance, as taught by Kuritani et al., would have been readily recognized in the component package of Kiyooka et al. for performing the same functions.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add an inorganic filler to the thermosetting resin of Kiyooka et al. in order to enhance thermal conductivity for drawing heat away from the embedded components, and to match the CTE of the thermosetting resin with that of the components to ensure the integrity and reliability of the component connections through the heat cycles of operation in the package of Kiyooka et al., as taught by Kuritani et al.

As to Claim 38, modified Kiyooka et al. further discloses an inner via 55 formed in the resin 36 that forms the insulating substrate 38 and electrically connected to the wiring patterns (37, 45) (Figs. 6b,c; p.3, final paragraph, lines 5-11).

As to Claim 39:

I. Kiyooka et al., as modified by Kuritani et al., teaches an insulating substrate formed of a mixture comprising a thermosetting resin combined with an inorganic filler that enhances thermal conductivity of the resin and modifies the CTE of the resin so that it matches that of the components in order to ensure reliable package performance.

II. Kuritani et al. further teaches that 70 wt % to 95 wt % of the mixture comprises the inorganic filler (p.6, lines 22-25; p.7, lines 10-29)--in the example on p.7, the mixture comprises 950/1109 = 86 wt % of the mixture--in order to obtain the above-cited properties of the resin with filler.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify the use of inorganic filler with the resin by formulating the mixture such that 70 wt % to 95 wt % of the mixture comprises the inorganic filler in order to enhance the thermal conductivity of the resin and modify the CTE of the resin so that it matches that of the components to ensure reliable package performance.

As to Claim 40, modified Kiyooka et al. further discloses the wiring patterns (37, 45) are formed on the principal plane and in an internal portion of the insulating substrate (Figs. 1e and 2; the sentence bridging pp.1-2 and p.2, lines 6-10).

As to Claim 41, modified Kiyooka et al. further discloses the inner via 55 is formed of a conductive resin composition 56 (p.3, final paragraph, lines 7-11).

As to Claim 42, modified Kiyooka et al. further discloses, in Fig. 2, the circuit component (33a,b,c and 42a,b) is shielded from external air by the insulating substrate (38, 46).

As to Claim 43, modified Kiyooka et al. further discloses the thermosetting resin (36, 44) comprises an epoxy resin (p.1, final paragraph, lines 1-5; p.2, first full paragraph, lines 1-5).

As to Claim 44, Kiyooka et al., as already modified by Kuritani et al. (base Claim 37), discloses that the inorganic filler is one of Al_2O_3, AlN and SiO_2 (Kuritani, p.6, lines 15-19).

As to Claim 46, modified Kiyooka et al. further discloses the wiring patterns (37, 45) comprise a conductive resin composition (the sentence bridging pp.1-2 and p.2, lines 6-10).

As to Claim 48, modified Kiyooka et al. further discloses the at least one component 33a is a passive component (either a capacitor, resistor or inductor; see Figs. 2 and 9).

As to Claim 52 (depending from either of Claims 41 and 46 which provide the antecedent basis for "the conductive resin composition"):

I. Modified Kiyooka et al. discloses that the conductive resin composition comprises silver particles (the sentence bridging pp.1-2 and p.3, final paragraph, lines 7-11).

II. Since modified Kiyooka et al. already uses an epoxy resin (36, 44) for the insulating substrate (38, 46) (p.1, final paragraph, lines 1-5), then the use of an epoxy

resin as the resin component of the conductive resin would have been readily recognized in the pertinent art of Kiyooka et al., at least because the material similarity between the epoxy resin of the insulating substrate and an epoxy resin for the conductive resin would facilitate CTE matching of the via filler 56 and wiring patterns (37, 45), with the insulating material (36, 44) of the insulating substrate (38, 46), thus enhancing package reliability during operational heat cycles.

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to also use an epoxy resin as the resin component in the conductive resin composition 56 in the via, as well as in the conductive resin composition used for the wiring patterns (37, 45), in Kiyooka et al. for at least the purpose of enhancing package reliability during operation.

Allowable Subject Matter

14. Claim 50 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 50, patentability resides in the limitation wherein the insulating substrate has **the combination of** *a coefficient of linear expansion of 8 ppm/°C to 20 ppm/°C* **and** *a heat conductivity of 1W/mK to 10W/mK*, in combination with the other limitations of the claim.

16. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tokuno (US 5,869,886) discloses a conductive epoxy resin 8 for electrically connecting a semiconductor chip 1 to a ground pattern 7 on a circuit substrate 6, wherein the conductive epoxy resin 8 comprises metal particles selected from the group consisting of silver, copper, palladium, silver palladium (col.3: 27-35; col.4: 39-50; col.5: 52-54).

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
November 05, 2005